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EXAMINER

KEBEDE, BROOK

ART UNIT PAPER NUMBER

2823

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/678,414

Applicant(s)

CARLSON, DAVID W.

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 March 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,5-7,9,10 and 13-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-7,9,10 and 13-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on March 25, 2002 in Paper No. 6 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claim 1 recites the limitation “chemically-mechanically polishing the layer of second material and the underlying layer of first material **with slurry** until the layer of second material is all removed from the layer of first material **without changing the slurry** to form the planarized layer of material” in lines 10-12. However, there is not support for, newly added limitation, **without changing the slurry** in the specification as originally filled. Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

2. The corrected or substitute drawings were received on March 25, 2002 in Paper No. 5. These drawings are acceptable. Accordingly, the drawing objection under 37 CFR 1.83(3) that was set forth in Paragraph 1 of Office action that was mailed on December 19, 2001 in Paper No. 4 is withdrawn.

Claim Objections

3. Claim 16 is objected to because of the following informalities:

Claim 16 recites the limitation “The method of claim 3 wherein the layer of first material makes an electrical contact with a device on wafer” in lines 1-2. However, claim 3 is cancelled by amendment of Paper 6. Therefore, dependency of claim 16 on claim 3 is improper. Applicant

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is advised either to change dependency of claim 16 or cancel the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 2, 5-7, 9, 10 and 13-17 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites the limitation “chemically-mechanically polishing the layer of second material and the underlying layer of first material **with slurry** until the layer of second material is all removed from the layer of first material **without changing the slurry** to form the planarized layer of material” in lines 10-12. However, there is not support for, newly added limitation, **without changing the slurry** in the specification as originally filled. Therefore, the subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 2, 5-7, 9, 10 and 13-17 are also rejected as being dependent of the rejected independent base claim.

6. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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Claim 20 recites the limitation “wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal or greater than the minimum thickness” in lines 2-5. There is no quantitative measurement that indicates the structure has a thickness ranges (i.e., minimum thickness) in the specification. Therefore, the limitation was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 5, 13 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation “wherein the layer of first material is formed such that the first lower level lies above the wafer above level by a value that equal or grater than the thickness” in lines 4-5. However, the recited limitation lacks clarity in its scope and meaning. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation “wherein the layer of first material is formed such that the first lower level lies above the wafer above level by a value that equal or grater than the thickness” in lines 4-5. However, the recited limitation lacks clarity in its scope and meaning. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Claim 20 recites the limitation “wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal or greater than the minimum thickness” in lines 2-5. However, the recited limitation lacks clarity in its scope and meaning. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Applicant’s cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 1, 2, 6, 7, 14-16, 18, 19, 21 and 23 rejected under 35 U.S.C. 102(b) as being anticipate by Doan et al. (US/5,618,381).

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Re claims 1 and 16, Doan et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material (22) on the top surface of the wafer, the layer of first material (22) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (22); and chemically-mechanically polishing the layer of second material (60) and the underlying layer of first material (22) with a slurry until the layer of second material (60) is all removed from the layer of first material (22) without changing the slurry to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 1-3, 6 and 7 and Col. 2, lines 7-67 through Col. 5, lines 1-34).

Re claim 2, as applied to claim 1 above, Doan et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 1-3, 6 and 7).

Re claim 6, as applied to claim 1 above, Doan et al. disclose all the claimed limitations including the limitation the first material as being polysilicon (see Col. 2, lines 26-29).

Re claim 7, as applied to claim 1 above, Doan et al. disclose all the claimed limitations including the limitation the second material is being an oxide (see Col. 4, lines 11-14)..

Re claim 14, as applied to claim 1 above, Doan et al. disclose all the claimed limitations including the limitation the step of doping the layer of first material prior to forming the layer of second material (see Col. 2, lines 26-29).

Re claim 15, as applied to claim 1 above, Doan et al. disclose all the claimed limitations including the limitation wherein the layer of first material is doped polysilicon (see Col. 2, lines 26-29).

Re claim 18, Doan et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material; and chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer (see Figs. 1-3, 6 and 7 and Col. 2, lines 7-67 through Col. 5, lines 1-34).

Re claim 19, as applied to claim 18 above, Doan et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 1-3, 6 and 7 and Col. 2, lines 7-67 through Col. 5, lines 1-34).

Re claim 21, as applied to claim 18 above, Doan et al. disclose all the claimed limitations including the limitation wherein the first material is doped polysilicon (see Figs. 1-3, 6 and 7 and Col. 2, lines 7-67 through Col. 5, lines 1-34).

Re claim 23, as applied to claim 18 above, Doan et al. disclose all the claimed limitations including the limitation wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 1-3, 6 and 7 and Col. 2, lines 7-67 through Col. 5, lines 1-34).

12. Claims 1, 2, 5-7, 10, 13-16 and 18-23 rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (US/6,162,368).

Re claims 1 and 16, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) without changing the slurry to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 2, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 5, as applied to claim above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

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Re claim 6, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the first material as being polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 7, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the second material is being an oxide (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 10 as applied to claim 2 above, Li et al. disclose all the claimed limitations including the limitation step of forming a layer of third material on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 13, as applied to claim 12 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 14, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the step of doping the layer of first material prior to forming the layer of second material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 15, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 18, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material on the top surface of the wafer, the layer of first material having

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a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material; and chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 19, as applied to claim 18 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 20, as applied to claim 19 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of first material has a thickness over the wafer upper layer, and wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 21, as applied to claim 18 above, Li et al. disclose all the claimed limitations including the limitation wherein the first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 22, as applied to claim 18 above, Li et al. disclose all the claimed limitations including the limitation forming a layer of third material on the planarized layer of first material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

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Re claim 23, as applied to claim 18 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. (US/5,618,381).

Re claim 9, as applied to claim 1 above, Doan et al. disclose all the claimed limitations. Regarding the first and second layers of material are chemically mechanically polished with a slurry that has a selectivity that falls within an approximate range of 0.9-1.1:1, the Examiner takes an Official notice since CMP process involves the introduction of a chemical slurry to facilitate higher removal rates and selectivity between films of the semiconductor surface such selectivity depends the composition of the slurry and the material that being removed and it is well-known in the art to determine the selectivity range of 0.9-1.1:1 given Doan et al. disclosure. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942). See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 17, as applied to claim 1 above, Doan et al. disclose all the claimed limitations. Although the relative thickness range of the first and second material within the scope of Doan et al. disclosure, Doan et al. do not specifically disclose the second material is approximately two to

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three times as thick as the layer of first material. However, this thickness range can be achieved by one of ordinary skill in the art at desired thickness range by routine experimentation. Generally, differences in concentration or temperature or thickness of the film will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature or particular thickness range is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Response to Arguments

15. Applicant's arguments with respect to claims 1, 2, 5-7, 9, 10, 13-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
June 2, 2002

Long Pham
LONG PHAM
PRIMARY EXAMINER